CLAIMS

What is claimed is:

1. A system, comprising:

a bus;

first logic to generate a multiphase encoded waveform; and

second logic coupled to the first logic to drive the multiphase encoded waveform onto the bus.

2. The system of claim 1 wherein the first logic includes a multiphase phase lock loop to generate multiple phases for the multiphase encoded waveform.

3. The system of claim 1 wherein second logic includes third logic to generate differential signal levels representing the multiphase encoded waveform.

4. The system of claim 2 wherein the first logic includes an input register, coupled to the multiphase phase lock loop, to receive at least one data word or at least one command/control word.

5. The system of claim 4 wherein the input register comprises a first-in-first-out (FIFO) register.

6. The system of claim 4 wherein the input register includes a command/control signal input, wherein a command/control signal on the command/control signal input is to indicate whether the multiphase encoded waveform is a data structure or a command/control structure.

7. The system of claim 3 wherein the bus includes at least one differential transmission line to receive signal levels for the multiphase encoded waveform.

8. The system of claim 7 wherein second logic further comprises impedance matching circuitry to match impedance of the second logic to the differential transmission line.

9. The system of claim 1, further comprising third logic coupled to the bus to receive the multiphase encoded waveform.

10. The system of claim 9 wherein the third logic includes an amplifier to receive differential signal levels representing the multiphase encoded waveform from the bus and extract the multiphase encoded waveform from the received differential signal levels.

11. The system of claim 10 wherein the third logic includes a differential delayed lock loop coupled to stretch a multiphase encoded waveform timing to a predetermined length.

12. The system of claim 11 wherein the third logic includes a register coupled to check data integrity of the multiphase encoded waveform.

13. An apparatus, comprising:

a device driver having first logic to generate a multiphase encoded waveform and second logic coupled to the first logic to drive the multiphase encoded waveform onto a bus.

14. The apparatus of claim 13 wherein the first logic includes a multiphase phase lock loop to generate multiple phases for the multiphase encoded waveform.

15. The apparatus of claim 13 wherein second logic includes third logic to generate differential signal levels representing the multiphase encoded waveform.

16. The apparatus of claim 14 wherein the first logic includes an input register, coupled to the multiphase phase lock loop, to receive at least one data word or at least one command/control word.

17. The apparatus of claim 14 wherein the input register comprises a first-in-first-out (FIFO) register.

18. The apparatus of claim 15 wherein the input register includes a command/control signal input, wherein a command/control signal on the command/control signal input is to indicate whether the multiphase encoded waveform is a data structure or a command/control structure.

19. The apparatus of claim 13 wherein second logic further comprises impedance matching circuitry to match impedance of the second logic to a bus differential transmission line.

20. An apparatus, comprising:

a device driver to receive a multiphase encoded waveform, having:

an amplifier to receive differential signal levels representing the multiphase encoded waveform from the bus and extract the multiphase encoded waveform from the received differential signal levels; and

a differential delay-lock loop coupled to stretch the received multiphase encoded waveform timing to a predetermined length.

21. The apparatus of claim 20, further comprising a register coupled to check data integrity of the received multiphase encoded waveform.

22. The apparatus of claim 21 wherein the register includes logic to extract data bits from the received multiphase encoded waveform and to perform a probability analysis to determine a likelihood of errors.

23. The network of claim 20 wherein the differential delay-lock loop includes logic to align rising edges of the received multiphase encoded waveform to rising edges of a transmitted multiphase encoded waveform.